CLEAN VERSION

IN THE SPECIFICATION

The title has been amended to read:

A1

--MOS TRANSISTOR USING MECHANICAL STRESS TO CONTROL SHORT CHANNEL EFFECTS--

The paragraph starting at page 1, line 5 has been amended to read:

A2

[0001] This is a divisional application of Serial No. 09/342,030 filed June 28, 1999, now U.S. Patent 6,362,082.

CLEAN VERSION OF PENDING CLAIMS

A3

1. A transistor device, comprising:

a substrate having a source region, a drain region and a channel region, in which at least one of the source, drain and channel regions has a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress; and

a gate region formed over the channel region.

2. The transistor of claim 1 wherein the void is located substantially in a center of the channel region.

3. The transistor of claim 1 wherein the void is approximately 50 nm across.

4. The transistor of claim 3 wherein the void is located at a depth of approximately 1000 angstroms in the channel region.

5. Please cancel claim.

6. The transistor of claim 1 wherein the void is located in the channel region and near an edge of the channel region adjacent to the source region.

7. The transistor of claim 1 wherein the void is located in the channel region near an edge of the channel region adjacent to the drain region.

8. A transistor, comprising:

a substrate having a source region, a drain region and a channel region, in which a void is located below the source region to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress; and

a gate region above the channel region.

9. The transistor of claim 8 wherein a void is also located below the drain region.

10. The transistor of claim 9 wherein the source and drain regions are under compressive stress.

11. The transistor of claim 8 wherein the source region is under tensile stress.

12. The transistor of claim 8 wherein the drain region is under compressive stress.

13. The transistor of claim 8 wherein the gate region is polysilicon.

14. The transistor of claim 8 wherein the gate region is metal.

15. A transistor comprising

a substrate having a source region, a drain region and a channel region; and.

a gate region having a void to place the substrate under mechanical stress to alter carrier mobility due to the stress.

16. Please cancel claim.

17. The transistor of claim 15 wherein the gate region is polysilicon.

18. The transistor of claim 15 wherein the gate region is metal.